AMENDMENT TO THE CLAIMS

1. (currently amended): A hard macro having an antenna rule violation free input/output port, comprising:

an input/output (I/O) port having a port level metallic conductor in a low level metalization layer;

an I/O transistor having a gate conductor separated from a diffusion region by a gate oxide layer;

a top level metallic conductor of a highest level metalization layer that is electrically coupled to a diffusion region; and

an electrical connection between the port level metallic conductor and the gate conductor including a first conducting section extending from the gate conductor to the top level metallic conductor and a second conducting section extending from the top level metallic conductor to the port level conductor;

wherein the I/O port is free of antenna rule violations, and the I/O port, the I/O ~~transmitter~~transistor, the top level metallic conductor, and the electrical connection form a predefined circuit element that is droppable into a floor plan of a circuit design.

2. (original): The hard macro of claim 1, wherein the first and second conducting sections include a plurality of vias extending vertically between adjacent metalization layers.

3. (original): The hard macro of claim 1, wherein the hard macro is selected from a group consisting of a processor, memory, an input interface circuit, an output interface circuit, an encoder, and a decoder.

4. (original): An integrated circuit including a plurality of the hard macros of claim 1.

5. (previously presented): A method of defining a hard macro having an antenna rule violation free input/output port, comprising steps of:

(a) defining an input/output (I/O) port having a port level conductor in a low level metalization layer;

(b) defining an I/O transistor having a gate conductor separated from a diffusion region by a gate oxide layer;

(c) defining a top level metallic conductor in a highest level metalization layer that is electrically coupled to a diffusion region;

(d) defining a first conducting section of an electrical connection extending from the gate conductor to the top level metallic conductor; and

(e) defining a second conducting section of the electrical connection extending from the top level metallic conductor to the port level conductor;

wherein the defined I/O port is free of antenna rule violations, and the defined I/O port, transistor, top level metallic conductor, and electrical connection form a predefined circuit element that is droppable into a floor plan of a circuit design.

6. (new): An integrated circuit including a plurality of hard macros, each hard macro comprising:

an input/output (I/O) port having a port level metallic conductor in a low level metalization layer;

an I/O transistor having a gate conductor separated from a diffusion region by a gate oxide layer;

a top level metallic conductor of a highest level metalization layer that is electrically coupled to a diffusion region; and

an electrical connection between the port level metallic conductor and the gate conductor including a first conducting section extending from the gate conductor to the top level metallic conductor and a second conducting section extending from the top level metallic conductor to the port level conductor;

wherein the I/O port is free of antenna rule violations, and the I/O port, the I/O transistor, the top level metallic conductor, and the electrical connection form a predefined circuit element that is droppable into a floor plan of a circuit design.